FT816 Floating Point Accelerator

Overview:

FT816 floating point accelerator consists of two ninety-six bit floating point accumulators between which floating point operations occur. Basic operations include ADD, SUB, MUL, DIV, FIX2FLT, FLT2FIX, SWAP, and NEG.

Floating Point Representation:

The floating point representation is triple precision (3x a 32 bit float) and consists of a 16 bit exponent, and eighty bit mantissa.

|  |  |
| --- | --- |
| 95 80 | 79 0 |
| SEEEEEEEEEEEEEEE | SM.MMMMMM………MMMMMMMM |

Range

Exponent ranges from -32768 to + 32767. The range is represented based at zero.

|  |  |  |  |
| --- | --- | --- | --- |
| SEEEEEE…. field | Exponent |  |  |
| FFFF | 32767 | maximum exponent |  |
| … |  |  |  |
| 8000 | 0 |  |  |
| … |  |  |  |
| 0000 | -32768 |  |  |

There are 79 bits in the mantissa plus a sign bit. So the range is -2^79 to +2^79 (approximately 24 digits of precision). The mantissa is represented in two’s complement form.

Operations Supported

Floating point calculations are performed by loading the floating point accumulators with values then setting an operation code in a command register.

|  |  |  |
| --- | --- | --- |
| Operation | Opcode |  |
| ADD | 1 | FAC1 = FAC1 + FAC2 |
| SUB | 2 | FAC1 = FAC1 – FAC2 |
| MUL | 3 | FAC1 = FAC1 \* FAC2 |
| DIV | 4 | FAC1 = FAC1 / FAC2 |
| FIX2FLT | 5 | FAC1 = convert to float(FAC1) |
| FLT2FIX | 6 | FAC1 = convert to fixed(FAC1) |
| NEG | 16 | FAC1 = -FAC1 |
| SWAP | 17 | FAC1 is swapped with FAC2 |
|  |  |  |

After the opcode is set in the command register, the operation status may be read from the status register. The most significant bit of the status register indicates a busy status.

Registers

Registers are mapped into the memory space of the system. The default is to map registers between $FEA200 and $FEA2FF. This mapping is controllable by optionally setting a parameter for the core.

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
| $FEA200 | FAC1 LSB of manitssa |  |  |
| … |  |  |  |
| $FEA209 | FAC1 MSB of mantissa |  |  |
| $FEA20A | FAC1 LSB of exponent |  |  |
| $FEA20B | FAC1 MSB of exponent |  |  |
|  |  |  |  |
| $FEA20F | Command / status register |  |  |
|  |  |  |  |
| $FEA210 | FAC2 LSB of manitssa |  |  |
| … |  |  |  |
| $FEA219 | FAC2 MSB of mantissa |  |  |
| $FEA21A | FAC2 LSB of exponent |  |  |
| $FEA21B | FAC2 MSB of exponent |  |  |
|  |  |  |  |